Mapping Deformation Fields in Integrated Circuit Metallization

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The availability of high brilliance synchrotron sources and focusing x-ray optics have facilitated the measurement of local parameters, such as composition, topology, stresses and strains in domains that are micrometers or smaller in size. Since the features of interest in microelectronics fall within this range, microbeam techniques are frequently used in analyzing ULSI devices. Currently there are three approaches that are utilized for deformation analysis. The first two are similar to the macroscopic techniques that are used in bulk measurements and use the spacing of atomic planes to determine strains in various directions. These strains are then transformed to get the strain and stress in the sample coordinates. The primary difference between these two techniques is the diffraction method; one uses monochromatic diffraction, the second, white beam Laue diffraction. The third technique utilizes topographic mapping of a strong reflection from the substrate, and yields relative stress/strain contours. These techniques yield complementary data, and should be used together where possible. Unfortunately, this is not a trivial task since the instrumental requirements for the techniques are significantly different. In addition, the theoretical basis of the measurements are not fully worked out at the present time.

In this talk, I will discuss. topographic determination of stress/strain and interface integrity in various samples, including real-time stress/strain changes in thin-film wires undergoing electromigration. I will also compare topographic data with high-resolution microdiffraction results to illustrate the complimentary nature of these techniques.